Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT 1**
2. **INPUT 1-**
3. **INPUT 1+**
4. **V-**
5. **INPUT 2+**
6. **INPUT 2-**
7. **OUTPUT 2**
8. **V+**

**.098”**

****

**.067”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: -V or FLOATING**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .067” X .098” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .020” P/N: HA0-5112-2**

**DG 10.1.2**

#### Rev B, 7/1